CHAPTER 1

1. Components of a computer: ALU and Control Unit (CPU), Memory, Input, and Output.

2. Functions of various components:

   .CPU: It processes and stores binary data, transfers data from and to memory and I/O devices, and provides timing to all the operations. It includes ALU, register arrays, and control unit. The ALU performs the arithmetic and logic operations, and the control unit provides timing.

   .Input - provides binary data as an input to the CPU.

   .Output - accepts binary data from the CPU.

3. A microprocessor functions as the CPU of a microcomputer, and includes the ALU, register arrays, and the control unit on one chip; it is manufactured using the LSI technology. On the other hand, the CPU is designed with various discrete boards. Functionally, both are similar; however, technology and processes used for designing is different.

4. A microprocessor is one component of a microcomputer, and the microcomputer is a complete computer consists of a microprocessor, memory, input, and output.

5, 6. See Summary: Scale of Integration

7. Four bytes.

8. The machine language of the 8085 are the commands to the microprocessor given in binary. These are the binary instructions the processor can understand and execute. The assembly language comprise of mnemonics (group of letters to represent commands) assigned by the manufacturer for the convenience of the users.

9, 10, 11. See Summary: Computer Languages

12. The assembly language mnemonics represent instructions to the microprocessor; therefore, when they are translated into machine language, there is one-to-one correspondence between the mnemonics and the machine code. The assembly language programs are compact, require less memory space, and are efficient. The high level languages are written in English- like statements, and when these statements are translated in machine language, the object code tends to be large, and requires large memory. The execution of the programs written in high level languages is less efficient than that of assembly language programs.

15, 16. See Summary: Computer Languages

15. ASCII codes in Hex: A = 41, Z = 5A, and m = 6D

16. See Summary: Computer Languages

CHAPTER 2

1. Memory Read, Memory Write, I/O Read, and I/O Write.

2. A bus is group of lines (wires or conductors) which carry digital information.

3. The function of the address bus is to carry a binary address of a memory location or an I/O device. The address bus is unidirectional, and the information flows from the MPU to peripherals and memory.

4. A microprocessor with 14 address lines is capable of addressing 16 K (2^{14}) memory locations.

5. 21 address lines.

6. Data bytes are transferred in both directions between the MPU and memory/peripherals.

7. IOR (I/O Read), IOW (I/O Write), MEMR (Memory Read), and MEMW (Memory Write).

8. In memory write operation, the control signal required is MEMW, and the direction of the data flow is from the MPU to memory.

9. The accumulator is an 8-bit register and it is a part of the ALU. All 8-bit arithmetic and logic operations are performed in relation to the accumulator content, and the result is stored in the accumulator (with a few exceptions).

10. A flag is the output of a given flip-flop to indicate certain data conditions.

11. The program counter and the stack pointer store memory addresses of 16 bits.

12. The program counter always points to the next memory location; therefore, the content of the program counter will be 2058H.

13. 128 registers and 128 X 4 = 512 memory cells.

14. 1024 bits are can be stored by this chip; however, it can not be specified as a 128-byte memory chip because the byte indicates 8-bit memory registers; this chip has 4-bit registers.

15. 8-bit word size.

16. 8 chips.

17. 4 chips.

18. 32 chips.

19. The WR signal enables the input buffer of a memory chip so that information can be stored (written) in the selected memory register.

20. 11 address lines.

21. 16 pages and the last location is 2FFFH.

22. The starting address is F800H, and the memory map is F800H to FBFFH.

23. The starting address is: E000H.

24. The address ranges from FF00H to FFFFH.

25. The address of the selected register: 1000 0000 0100 0111 = 8047H

26. The memory map ranges from 2000H to 23FFH.

27. The address of the selected register: 0010 0000 1111 1000 = 20F8H

28. 8 address lines are required for a peripheral I/O port, and 16 address lines are required for a memory-mapped I/O port.

29. Tri-state devices are logic devices with three states; the third state is high impedance. In a bus-oriented system, devices are connected in parallel, and the buses are capable of driving one TTL logic device. The MPU communicates with one peripheral at a time, and other peripherals are placed in high impedance to avoid bus loading.

30. High impedance state.

31. From B to A.

32. None. The decoder is not enabled; all output lines will be high.

33. The line 6 (O_6)

34. 0 0 1 (Complement of 1 1 0)

IO/M	RD	WR	Output Signal		
0	0	0	O_0	Invalid	RD and WR cannot be active simultaneously
0	0	1	O_1	MEMR	M and RD active
0	1	0	O_2	MEMW	M and WR active
0	1	1	O_3	Irrelevant	Both RD and WR are inactive
1	0	0	O_4	Invalid	RD and WR cannot be active simultaneously
1	0	1	O_5	IOR	IO and RD active
1	1	0	O_6	IOW	IO and WR active
1	1	1	O_7	Irrelevant	Both RD and WR are inactive

4. See the answer of Q.3.

5. In Fig. 3.23, the 74LS139 is enabled when IO/M is low. Therefore, the following memory control signals can be generated.

RD	WR	Decoder Output
0	0	O_0 - Invalid
0	1	O_1 - MEMR
1	0	O_2 - MEMW
1	1	O_3 - No operation

6. The output of the latch will be 05H; however, it will be not be latched until the ALE goes low.

7. The output of the latch is 05H. At T2, the ALE is low; therefore, the latch will not be enabled, and it will continue to hold the previously latched byte (05H).

8. The crystal frequency should be = 2.2 MHz because the oscillator logic divides the input frequency by two.

9. See the steps on page 66/67, Example 3.1.

10. The sum of 87H + 79H = 100H. Therefore, the accumulator will have 00H, and the flags will be S = 0, CY = 1, Z = 1.

11. 2060H. The program counter always points to the next machine code to be fetched.

12. 18T X .2 micro-sec = 3.6 micro-sec.

13. (A15-A8) = 20H, (AD7-AD0) = 47H, (PC) = 2076H

14. RD and IO/M are asserted low.

```
0085 =          BYTE2   EQU   85H
00F3 =          PORT    EQU   0F3H
201C                    END
```

43. This program turns on the LED indicator when the switch S7 is on.

```
2000                    ORG 2000H
2000 DBF1       START:  IN 0F1H       ;Comments are same as  illustrative
2002 47                 MOV B,A       ;program -- omitted here
2003 DBF2               IN 0F2H
2005 E680               ANI 80H
2007 4F                 MOV C,A       ;Save S7'
2008 78                 MOV A,B       ;Get data from port F1
2009 E680               ANI 80H
200B CA1420             JZ  TURNON    ;If S7 =0, turn on belts
200E D3F3               OUT 0F3H      ;Turn on LED to indicate S7 is on
2010 A1                 ANA C         ;Check S7 and S7'
2011 C21C20             JNZ SHTDWN
2014 78         TURNON: MOV A,B
2015 E61F               ANI 1FH
2017 D3F3               OUT 0F3H
2019 C30020             JMP START
201C 3E40       SHTDWN: MVI A,40H     ;Load byte to turn off belts and turn on emergency
201E D3F3               OUT 0F3H
2020 76                 HLT
                        END
```

CHAPTER 7

The following programs assume the systems R/W memory begins at location 2000H. The symbols XX in the assignments are assumed as memory page 20H.

Section 7.1

See Figures 7.1, 7.2, 7.3, & 7.4: pg. 81

Section 7.2

5. Location 2075H will contain F7H

```
        MVI B, COUNT1 ;Count for 200  s pulse      7
LOOP1:  DCR B                                      4
        JNZ LOOP1                                  10/7
        MVI A, 00H    ;Bit pattern to turn off D0  7
        OUT PORT1     ;Off-period begins           10
        MVI B, COUNT2 ;Count for 400  s delay      7
LOOP2:  DCR B                                      4
        JNZ LOOP2                                  10/7
        JMP TURNON                                 10
```

On-period Delay:

T = To + T

200 = (24 T x 325.5 ns) + (14 T x 325.5 ns x COUNT1)

$$\text{COUNT1} = \frac{(200 - 7.81) \times 10}{(4.557 \times 10)} = 42$$

Off-period Delay:

T = To + T

400 = (34 T x 325.5 ns) + (14 T x 325.5 ns x COUNT2)

$$\text{COUNT2} = \frac{(400 - 11.06)}{(4.557 \times 10)} = 85$$

18.

```
START:   MVI L,10101010B   ;ALTERNATING LIGHT PATTERN
LIGHTS:  MOV A,L
         RRC
         OUT PORT
         MOV L,A
         MVI B,50          ;20 x 50 mSec DELAY = 1 Sec
OUTER:   LXI D,2559        ;20 mSec DELAY
INNER:   DCX D
         MOV A,D
         ORA E
         JNZ INNER
         DCR B
         JNZ OUTER
         JMP LIGHTS
```